REMARKS

In the Office Action, the examiner objected to the drawings on the ground that Figure 4 lacks a prior art legend. Accordingly, the applicant has submitted concurrently herewith a request for approval of drawing changes in which a "Prior Art" legend is added to Figure 4 as shown by red ink. A replacement sheet for Figure 4 is also enclosed.

The examiner objected to the claims on the ground that the recitation of the "data file" in Claims 9 and 19 does not accurately describe the limitation described in the specification which recites a "value change dump file". Accordingly, the application has amended Claim 9 and 19 to change the "data file" to the "value change dump file" to correct the informalities.

In the Office Action, the examiner rejected Claims 1-3, 6-7, 10-13 and 16-17 under 35 U.S.C. 103(a) as being obvious over the teachings by Rhim et al. (cited reference, U.S. Patent No. 6,006,022) in view of Pieper et al. (cited reference, U.S. Patent No. 5,371,851). Accordingly, the applicant has amended the set of claims for more clearly differentiate the present invention from the teachings in the cited references. The applicant believes that the present invention defined in the claims as amended cannot be obvious to one skilled in the art due to the teachings of any of the cited references.

The objective of the present application is to provide an effective method to validate a complex IC, typically, system-on-a-

chip (SoC) design by using silicon ICs and an event based test system (event tester). The context apparatus of the present application is an event tester which has an architecture different from any existing tester.

The existing IC test systems prior to 1998 and still today are cycle based test systems (cyclized testers) that use predefined waveforms (RZ, NRZ, EOR) for each test period or test cycle. Because of this cyclization, existing testers require that simulation vectors developed during the IC design be translated into a special cyclized format according to the particular tester format. For example, simulation vectors from a Verilog or VHDL simulator are translated into two popular cyclized formats, i.e., WGL or STIL format. Using these WGL/STIL vectors, test engineers develop a program for the tester (generally called a test program). This translation process often causes errors. Moreover, this translation as well as the test program development is also very time consuming and costly. Another drawback is that data in the design environment and in the test environment are in different format, hence, when an error is observed in the test environment, it requires considerable effort to identify what is wrong in the design environment.

To overcome these problems, the assignee conceived a new architecture of a test system that uses data in a event format (timed event data) instead of preset waveforms per test cycle. In timed event data, events are transitions such as 0-to-1 and 1-to-0

and time being either absolute time (ex. with reference to start of operation) or relative time (ex. with reference to previous event) of events. There is no notion of preset waveforms/cycle in the operation of event based test system. To the best of the applicant's knowledge, except the tester build by the assignee, such event based test systems do not exist. The benefit of this test system is that it eliminated the need for vector translation and test program development. As this test system works in the event format, the assignee called it an event based test system (or event tester).

The design and operation of an event tester was described by the assignee in the U.S. Patent No. 6,360,343 and U.S. Patent No. 6,532,561. The design as well operation of the event tester is fundamentally different from the design and operation of the present day testers (cyclized testers). The concept, operation and method to build an event based test system are taught only by the assignee in the patents mentioned above. Using this event tester, the assignee has developed a method for IC design validation, described in U.S. Patent Application No. 09/428,746 (this application was recently approved as U.S. Patent No. 6,678,645). This information is disclosed in the present application at page 10, lines 9 to 18.

In U.S. Patent Number 6,678,645, the assignee described a method of using a multiple event tester units to validate individual cores in a system-on-a-chip, first individually and then

in combination. In the present application, two new concepts for IC design validation have been disclosed using the event tester: (i) design validation using an event tester and a prototype silicon; (ii) deign validation on an event tester (without using any prototype silicon). These features are explained in the present application at page 10, lines 19 to 24.

It should be noted that the concepts described in U.S. Patent No. 6,678,645 as well as in the present application do not exist today because an event tester does not exist (except those event testers that are built by the assignee, which are currently not in the market). The present state of the art IC design validation is either: (a) validation using EDA simulators; (b) validation using emulators; or (c) validation using field programmable devices such as FPGAs. The above-described state of the art technology is also fully explained in the present application pages 3 to 6 with reference to Figures 2 and 4.

The cited Rhim et al. reference (U.S. Patent No. 6,006,022) describes the concept of design validation using field programmable devices such as FPGAs. It should be noted that this traditional method is explained in the present application as the state of the art (c) noted above including the hardware/software co-development procedure at page 6, lines 4-34. One of the essential feature of the present application is that the test method does not use any FPGA. In the first concept in the present application, as shown in Figure 5, the method uses a prototype IC (numeral 61 in Figure 5),

that implements the design itself; while in the second concept, as shown in Figure 6, no prototype IC is used at-all, the design files are validated directly on the event tester.

Therefore, the concept as well as the apparatus in the present application is fundamentally different from the context and apparatus of any of the cited references or practices available today. The use of event tester is essential for implementing the method of the present application. All of the independent claims (Claims 1, 9, 10 and 19) in the present application identify this requirement explicitly. The event based test system is a physical entity, an equipment/machine, apparatus required for the procedure described in our application. To clarify the meaning of event and event based test system of the present invention, the applicant has amended Claims 1, 9, 10 and 19 to add "where the event based test vectors are test vectors in an event format in which an event is any change in a signal which is described by its timing and the event based test system is a test system for testing an IC by utilizing the event based test vectors".

In the official action, the examiner has stated that Rhim el al. teach a method of validating design of complex integrated circuit (IC) under EDA system (Figs. 1-17 and its description). However, it is important to note that the concept disclosed in the cited Rhim et al. reference is a FPGA based implementation as already mentioned above and at page 6 of the present application as one of the conventional technologies.

Examiner has further mentioned that Rhim et al. teach a method of applying event based test vectors derived from the IC design data to the prototype silicon by an event based test system and evaluating the response output to the prototype silicon (Fig. 1 and its description). The applicants respectfully disagree with this assertion. There is no such notion in the cited Rhim et al. reference because it does not describe an event based test system at all. The event based test system was invented by the assignee in 1998, there was no notion of event based test system prior to that, subsequently, there cannot be any notion of the usage of such a test system.

The applicants failed to see the relevance of another cited reference, U.S. Patent No. 5,371,851 issued to Pieper et al. by itself or in combination with the cited Rhim et al. reference. Nonetheless, it is worth mentioning that the graphical editor described in the cited Pieper et al. reference is for a cyclized tester. The contribution of the cited Pieper et al. reference is a graphical means through which a user can edit the waveforms (select one or more preset waveforms) and some other test conditions, it can by no means be used to edit timed event data as used in the event test system (there is no notion of waveforms in event tester). Because the graphical editor in the cited Pieper et al. reference is for cyclized tester, it is also worth mentioning that the embodiment in this cited reference also describes data

translation as explained above, which is not required in the method of the present invention.

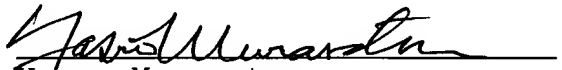
As noted above, significant differences exist between the present invention and cited references because the present invention. The applicant has amended the claims to more clearly specify these differences. Therefore, the applicant believes that the present invention is not obvious over the cited references taken singly or in combination.

In view of the foregoing, the Applicant believes that Claims 1-19 are in condition for allowance, and accordingly, the applicant respectfully requests that the present application be allowed and passed to issue.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 2/18/05

By: 

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IN THE DRAWINGS:

The applicant has submitted concurrently herewith a request for approval of drawing changes in which a "Prior Art" legend is added to Figure 4 as shown by red ink. A replacement sheet for Figure 4 is also enclosed.

Fig.4
(Prior Art)